Next-Generation Energy Harvesting Electronics: Holistic Approach
Workshop and Showcase
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Efficient and adaptive power electronics for Energy Harvesting

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System operation from cold start

- Energy Harvester
- Energy Storage
- Load Electronics

$V_{cap}$

No stored energy

$t$

$P_{load}$
System operation from cold start

- Energy Harvester
- Passive Start-up
- Energy Storage
- Load Electronics

$V_{cap}$

No stored energy

Load isolated

$t$
System operation from cold start

Energy Harvester → Passive Start-up → Energy Storage

Load isolated

Load Electronics

$V_{cap}$

$V_{th}$

$t$
System operation from cold start

Energy Harvester → Passive Start-up → Primary Power Converter → Energy Storage → Load Electronics

PWM

Ancillary Circuits

$V_{cap}$

$V_{th}$

$t$

Load isolated
System operation from cold start

- Energy Harvester
- Passive Start-up
  - Primary Power Converter
  - Energy Storage
  - Load isolated
    - Load Electronics
- PWM
- Ancillary Circuits

$V_{cap}$

$V_{on}$

$t$
System operation from cold start

Energy Harvester → Passive Start-up → Primary Power Converter → Energy Storage → Load Electronics

PWM

Ancillary Circuits

$V_{cap}$ vs. $t$

$V_{off}$
System operation from cold start

Energy Harvester → Passive Start-up → Primary Power Converter → Energy Storage → UVLO → Load Electronics

PWM
Ancillary Circuits

$V_{cap}$ vs $t$
3 cycles and their time scales

Voltage boosting ×10

Power boosting ×1000

Switched-mode conversion

Charge cycle: 60 s

V_in (AC)

Harvester cycle: 23 ms (44 Hz)

Harvester cycle averaged 75 μW

Switching cycle: 33 μs (30 kHz)

P_in averaged

P_out

V_out

V_in

V_out

V_in

V_out

V_in

50 mW
Low-power implementation

- Energy Harvester
- Passive Start-up
- Primary Power Converter
- Energy Storage
- UVLO
- Load Electronics
- PWM
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Low-power implementation

- **Energy Harvester**
- **Passive Start-up**
- **Primary Power Converter**
- **Energy Storage**
- **UVLO**
- **Load Electronics**
- **Ancillary Circuits**

**88 Hz alternating boost converters**
One switch at 30 kHz
Requires polarity detection

- **Stray L of harvester**
- **V\_in**

PWM implementation with 88 Hz alternating boost converters. One switch at 30 kHz, requiring polarity detection.
Low-power implementation

Passive Start-up

Energy Harvester

Primary Power Converter

PWM

Ancillary Circuits

Energy Storage

6-stage voltage multiplier

Voltage detector power-gates the µC
µC controls activation of ancillary circuits and isolates voltage multiplier via JFET isolation switches
Low-power implementation

Energy Harvester -> Passive Start-up -> Primary Power Converter -> Energy Storage -> UVLO -> Load Electronics

PWM to Ancillary Circuits
Low power implementations: useful ancillary circuits

**DAC**
- µC outputs active in low-power mode
- R2R matrix

**PWM**
- Quartz osc.
- Precision RC + comparator
- Jitter < 0.2%
  - max δ = 97%

**µC**
- LPM4 = 100 nA max clock frequency
- on once per 23 ms harvester cycle for 4 µs
- on once every 15 harvester cycles for 34 µs to track max power transfer:
- measure $I_{out}$, calculate direction, perturb $\delta$

**Gate drive**
- ULP logic gates
- Mosfets selected for low $R_{DS(on)}$ and $Q_{GS}$

$\Delta I_{out}$ measurement for max power transfer tracking
- Synchronised to harvester cycle
- 12 Hz low-pass filter: Low power OpAmp continuously on to avoid settling time
Comparing control techniques

Harvester output power (Utilisation drops with output power)

System Effectiveness (% Useful output power)

Max Potential Power (µW)

Conversion loss

Quiescent

Useful Output Power

Passive

Intermit.

Fixed $\delta$

$\eta > 70\%$

MPTT

H-bridge

Fixed $\delta$, $\eta > 70\%$
Options for adaptation

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Options for adaptation

- ac/DC
- P&O

Model

\[ P_{\text{in}} \rightarrow \text{ac/DC} \rightarrow P_{\text{out}} \]

Stored Energy (J)

Time (s)

Start up

MPTT

Open-loop

\( \delta = 0.67 \)

Passive Quadrupler

Excitation:

- 5 m·s\(^{-2}\)
- 4 m·s\(^{-2}\)
- 3 m·s\(^{-2}\)
- 2 m·s\(^{-2}\)
- 1.5 m·s\(^{-2}\)

Power averaged over output:

- 1.5 V < \( V_{\text{cap}} \) < 2.5 V

Output Current, \( I_{\text{use}} \) (\( \mu \text{A} \))

Time (s)

Duty Ratio, \( \delta \)
Slides for Q&A
Output Current, $I_{use}$ (μA)

$V_{out} = 4.5\text{V}$

$V_{out} = 2\text{V}$

Duty Ratio, $\delta$

Time (s)
Excitation:
5 m/s⁻²
4 m/s⁻²
3 m/s⁻²
2 m/s⁻²
1.5 m/s⁻²

Power averaged over output:
1.5 V < V_{cap} < 2.5 V

Normalized Output Power

Duty Ratio, δ
Main challenges

- Interface circuit design
- Matching circuit behaviour to harvester (impedances)
- Maximum power point tracking
- Tracking amplitude, frequency and load changes
- Very low power implementations
Interface Circuit Design

- Rectification and Voltage Boosting
  - The harvester generates low-amplitude (<1V) AC voltage
  - The load requires 2V – 4.5V DC voltage
- Zero energy start-up
Matching circuit input impedance to harvester

- Maximum power is extracted at matched impedances
- Harvester impedance is a function of the frequency
- Complex conjugate impedance matching requires high quiescent power for implementation
- Power close to the theoretical maximum can be extracted when the emulated resistance matches the magnitude of the source impedance

Power extracted with fixed load (green) and load adaptive to the frequency (blue)
Converter control

- The input impedance of the converter is a function of the instantaneous input and output voltages.
- For maximum power extraction, the impedance should be fixed during the harvester cycle and equal to the optimum.
**Maximum Power Transfer Tracking**

- The power delivered to the load is a function of the extracted power and the conversion efficiency.
- The optimum operating point is a function of the excitation magnitude and the output voltage.

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**Output power as a function of the duty ratio at different output voltages, acceleration is constant (200 mg)**

**Output power as a function of the acceleration averaged over output voltage levels from 1.5 to 2.5 V**
Low power implementation

- All functional requirements should be implemented at very low power which will allow for miniaturization of the harvester.
- To achieve low-power operation:
  - The quiescent consumption should be as low as possible.
  - The conversion efficiency should be maximised.

Implementation of high-efficiency ultra-low-power adaptive interface circuitry for energy harvesting.
Power electronics

Adaptive operation example:

• Acceleration of the input excitation: 3.75 m\(\cdot\)s\(^{-2}\)
• Charging 68 mF capacitor from 0 V to 3.3 V
• The digital control becomes operational at 1.8 V and MPTT finds the optimum duty-ratio
Power electronics

Adaptive operation example:

- Output power is a function of the input power and the efficiency of the converter.
- MPTT maximises the output power.
- Average overall efficiency (ratio between the output power $P_{\text{store}}$ and theoretical maximum power $P_{\text{max}}$) – 0.7-0.75%
Improving the adaptiveness of the system

- Instantaneous optimisation corresponding to variations of the input and output voltages – ensures the input resistance of the converter is not affected by variations of the input and output voltages
- Response to changes in the frequency of the excitation – the new optimum point can be determined by measuring the frequency

![Diagram of the system](image-url)
Constant resistance emulation

- Duty ratio required to maintain constant resistance during one cycle:

  - $V_{\text{in pk}} = 0.6 \, \text{V}$
  - $V_{\text{out}} = 2 \, \text{V}, 4.5 \, \text{V}$
  - Maximum variation of the required duty ratio: 17%
Fixed resistance emulation

- Emulated resistances for different output voltages with variable duty ratio compared to constant duty ratio

- Constant duty ratio results in 15% maximum deviation from the optimum resistance during the period of conduction
Magnitude matching

- Optimising the input resistance of the converter to match the magnitude of the source impedance.
Emulated Resistance

- Measured resistance (×) compared to the theoretical optimal resistance (−) for maximum power extraction with magnitude matching.
$|a| = 1.5 \text{ m.s}^{-2}$

$f = 43.6 \text{ Hz}$