

Experimental Investigation of Inductorless, Single-Stage Boost Rectification for sub-mW Electromagnetic Energy Harvesters

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Abstract—This paper demonstrates single-stage boost rectification for electromagnetic energy harvesters down to approximately 100 μW using practical low-power techniques. The circuits exploit the inductance of the generator, and operate without a discrete inductor, which facilitates integration. Experimental results demonstrate the importance of switching device selection, and the compound effect of the duty ratio on energy harvester output power and converter efficiency, as a function of load current. The circuits demonstrate up to 84.1% harvester utilization at the maximum extractable harvester power of 141 μW , and conversion efficiencies of 73.3% and 59.4% for half- and full-wave operation respectively, neglecting gate drive losses.

Keywords – Low power electronics, energy harvesting, AC-DC power converters, rectifiers

I. INTRODUCTION

Microscale, electromagnetic energy harvesters generate alternating currents, in most cases, at voltages below 2V [1]. Therefore rectification and boosting to a voltage level that permits compact energy storage in a capacitor is desirable (Fig. 1). Efficient converter topologies that perform rectification and voltage boosting must be designed with the characteristics of the generator in mind, by considering the interaction with the resonant system. The term harvester utilization describes how close to the optimum the harvester is loaded, and is defined as the ratio of the actual generated power to the maximum available power that is extracted when the load is matched to the output impedance of the generator [2]. The overall harvesting system efficiency is given as the product of the harvester utilization and the conversion efficiency of the interfacing power management circuit.

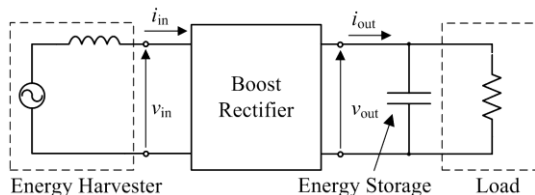


Figure 1. Elements of a simplified electromagnetic vibration energy harvesting system.

Rectification of the output current and boosting of the output voltage level is typically carried out in two separable stages [3][4], a rectifier circuit followed by an active voltage-conditioning topology. In the energy harvesting literature, reported topologies of this type demonstrate active rectification [5] at 85% efficiency, delivering an output voltage of 2.5 V at 25 μW , and DC-DC boost conversion [6] that

is around 75% efficient at 100 μW when boosting from 100 mV to 1 V. More recently, single-stage, direct AC-DC converter circuits have been proposed for energy harvesting applications [7][8]. For example, [9] demonstrates an actively switched split-capacitor direct AC-DC converter operating at an estimated 60% efficiency from a 400 mV_{peak} voltage at tens of milliwatts. These active topologies are implemented using a discrete inductor. In general, increasing the inductance provides a more efficient design with lower required switching frequency and ripple currents. By contrast, the circuits presented in this work use the parasitic stray inductance of the energy harvester, as this eliminates a component that is difficult to integrate. Well known in high-power applications, this concept has but recently been applied to energy harvesting [10][11]. The detailed discussion of the disadvantages of using the stray inductance of the coil, including poor quality factor, and limited circuit topologies, exceed the scope of this work.

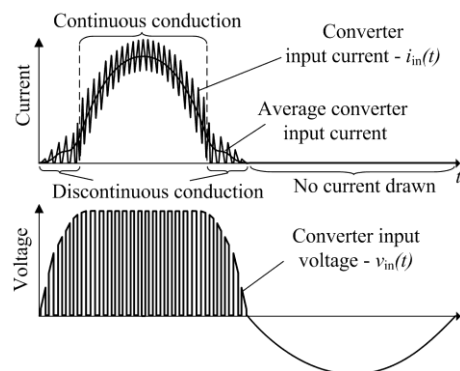


Figure 2. Conceptual harvester output voltage and current waveforms (power converter input waveforms) when using an active half-wave boost rectifier. The switching frequency has been reduced for clarity.

Fig. 2 depicts conversion during only the positive voltage cycle (half-wave operation), a technique that has been shown to provide a favorable power efficiency for certain energy harvester systems [12], due to the reduction in required gate drive power and control complexity and the reduced diode forward conduction loss. In this paper, practical realizations of both full- and half-wave boost rectifiers are presented to illustrate the differences in component power loss and harvester utilization.

Section II presents the electromagnetic harvester and the experimental setup. Section III shows results of passive rectification. Section IV reports the design of four active single-stage boost rectifier circuits exploring the achievable harvester utilization. Section V presents experimental results for the converter output power and converter efficiency, then the individual component losses are inferred as a function of system power for both half- and full-wave operation. Results are benchmarked against the theoretical maximum power that can be extracted by the optimum resistive load.

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II. ENERGY HARVESTER AND EXPERIMENTAL SETUP

The harvester used is a cantilever structure with a neodymium magnet used as a tip mass (Fig. 3). The harvester is 25 cm³ in volume has a resonance frequency of 59.4 Hz.

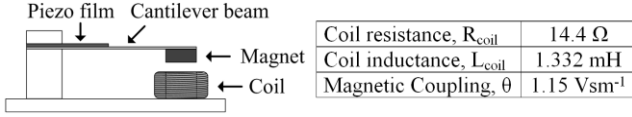


Figure 3. Electromagnetic harvester and its electrical characteristics.

The harvester frame is actuated by a shaker driven by an audio power amplifier (Fig. 4). This excitation is controlled by a dSPACE platform, keeping the magnitude of the frame acceleration constant, as measured by an accelerometer mounted on the middle of the harvester frame. The dSPACE system provides closed-loop acceleration control for the mechanical excitation, and measurement and data logging functions using ADCs, analogue control signals using the built in DAC module, and pulse-width modulation (PWM) signals for the active topologies. In cases, where a floating gate signal is required, a separate arbitrary waveform generator is used as the PWM source. The sampling frequency of dSPACE is limited to 10 kHz, therefore a 4-channel oscilloscope is used to capture the high frequency switching signals.

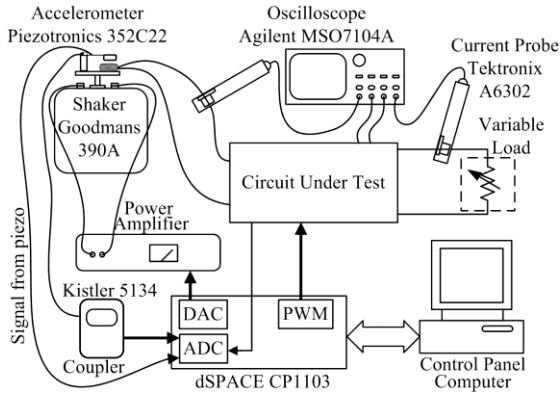


Figure 4. Experimental setup.

III. PASSIVE RECTIFICATION

A. Optimum resistive load and ideal half-wave rectification

Fig. 5 shows the measured harvester output power as a function of load resistance for three situations: 1) the resistor is connected directly to the output of the energy harvester without a reservoir capacitor, 2) the resistor isolated via a MOSFET during the negative output voltage half-cycle, and 3) the resistor is isolated during the positive half-cycle. The load resistance represents the apparent input impedance of an interfacing power management circuit. A maximum power of 1.42 mW is extracted using a 40 Ω load when the harvester is excited at its resonant frequency of 59.4 Hz with a constant acceleration of 6 m/s² in magnitude. The open circuit voltage at this excitation is 0.58 V_{rms}.

Interestingly, the half-cycle operation does not halve the output power, indicating that kinetic energy is being transferred from the unloaded to the loaded cycle. In this case, power is extracted not only at the fundamental frequency, but at its harmonics where the current sees a reduced harvester output impedance resulting in lower internal losses [12]. Therefore the difference between extracted power levels by ideal half- and full-wave operation is smaller than perhaps expected.

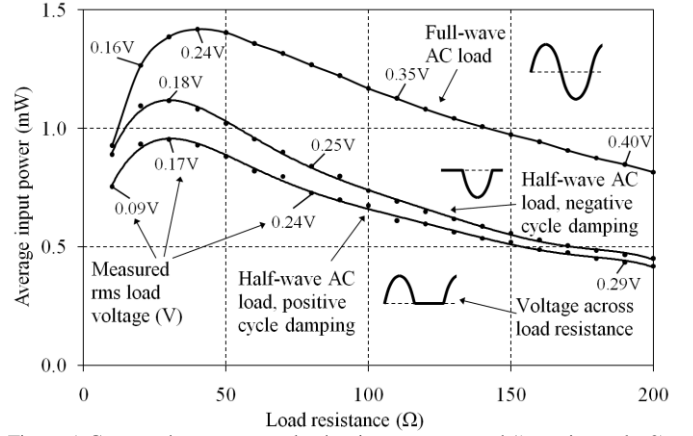


Figure 5. Generated power versus load resistance connected 1) continuously, 2) during positive output voltage half-cycle, and 3) during negative output voltage half-cycle. Fixed source excitation of 6 m/s² at 59.4 Hz.

Fig. 5 also demonstrates the asymmetric nature of the harvester transduction mechanism; the negative voltage cycle, which corresponds to the magnet's downward stroke, provides a higher harvester utilization than the positive cycle, and a maximum harvester output power of around 1.1 mW. All following half-wave rectification results relate to the negative voltage cycle.

B. Diode half- and full-wave rectification with DC smoothing

Passive rectifiers, shown in Fig. 6 a) and b), do not emulate an optimum load, and therefore harvester utilization is typically low.

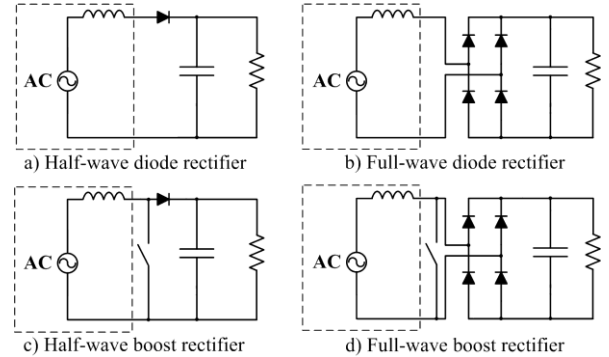


Figure 6. Passive rectifier and boost rectifier topologies.

Fig. 7 shows measured output power versus load resistance, for half- and full-wave Schottky-diode (1N5817) rectifier circuits with a 1 mF smoothing capacitor connected in parallel with the load resistance.

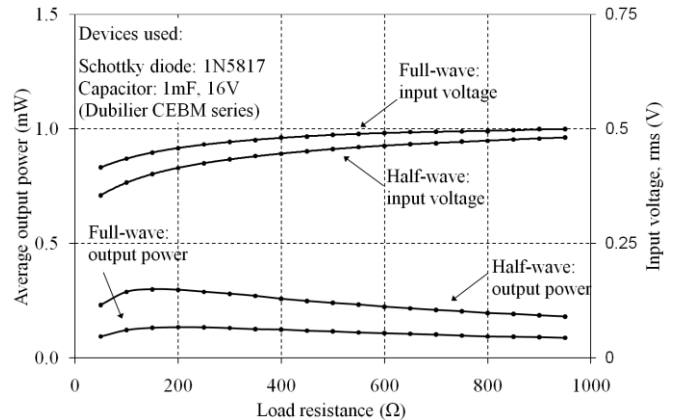


Figure 7. Output power and input voltage of passive full-wave (Fig. 6 a), and half-wave (Fig. 6 b) diode rectifiers feeding a stiff DC link, at fixed excitation of 6 m/s² at 59.4 Hz, and converter switching frequency of 32.768 kHz.

The advantage of the full-cycle loading of the harvester in terms of the maximum extracted power that was described in Section A is outweighed by the penalties of the additional diode conduction losses within the full-wave diode rectifier. The efficiency penalty due to the diode forward voltage drop is exacerbated by a low harvester voltage of 0.3–0.5 V. The utilization of the harvester is low for both half- and full-wave topologies at 20–40%. The measured conversion efficiency of the half-wave diode rectifier (55–65%) is significantly higher than that of the full-wave circuit (25–40%). This difference results in a significantly higher output power for the half-wave topology.

IV. ACTIVE INDUCTORLESS BOOST RECTIFICATION

A review of boost rectifier circuits is presented in [13]. These active topologies can be controlled, by adjusting parameters such as the switching frequency or the duty ratio, in order to emulate a desired apparent load impedance at the generator’s output, to maximize the extracted power [14]. Maximum power point tracking techniques have been demonstrated to achieve this [15]. At milliwatt power levels and higher, active boost rectifier topologies offer improved conversion efficiency over the passive topologies, with an acceptable quiescent power overhead of the control and gate drive circuitry [7].

The common boost converter topology consists of an inductor, a switch and a rectifying diode. During the on period, the switch is closed and the input current ramps up. When the switch turns off, the voltage across it rises until the diode becomes forward biased and begins conducting. At this point, energy is transferred from the inductor to the output capacitor. In boost rectifier circuits used here, (Fig. 6 c and d), the boost converter relies on the stray inductance of the coil for voltage boosting. A fixed switching frequency is used for simplicity. A suitable frequency lies around 30 kHz; high enough to result in acceptable input current ripple and thus low conduction losses, without causing excessive switching losses. In addition, this offers a conduction period that is below the L/R time constant, where the inductor current becomes strongly nonlinear. The frequency of the PWM output of dSPACE is set to 32.768 kHz, matching the output frequency of the off-the-shelf low power oscillator, OV-7604-C7.

A. Selection of Switch for Boost Conversion

An important part of the circuit design is the choice of the switching device. Whilst the full-wave circuit can extract power during both the positive and the negative half-cycles, in the half-wave case, the switch would ideally block current during the negative half-cycle, and thus keep the harvester open circuited, avoiding undesired damping. Four switching device options (Fig. 8) are considered; 1) a single n-channel JFET, 2) a single n-type MOSFET, 3) n-type MOSFET in series with a Schottky diode, and 4) two series-connected MOSFETs (bidirectional MOSFET).

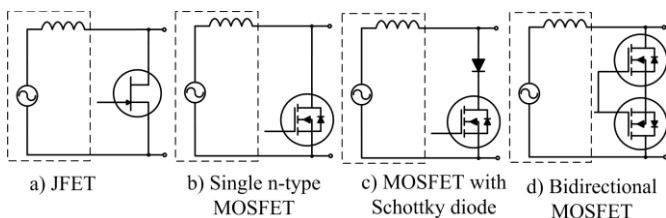


Figure 8. Investigated switch options for half-wave boost rectifier circuit.

The JFET (Fig. 8 a) is capable of blocking current in both directions when the channel is pinched off by reverse biasing the gate. In contrast, n-type MOSFETs (Fig. 8 b) do not block in the source-to-drain direction due to the inherent body-drain diode. A Schottky diode connected in series (Fig. 8 c) prevents the negative current flow at the expense of increased conduction losses during the periods when the switch is closed. P-channel devices typically have higher conduction losses than an equivalent size n-type MOSFET, therefore, two n-channel transistors are connected in a common source configuration

(Fig. 8 d). This allows a common reference for the gate signal for both devices but also means that the source, which is the zero volt reference for the gate drive cannot be connected to the ground of the load circuit.

TABLE I. IMPORTANT DEVICE PARAMETERS

Parameters	JFET – J106	MOSFET – SI-2302DS
Gate voltage, V_{GS}	-3.7 – 0 V	0 – 2 V
Capacitance, C_{iss}	160 pF	340 pF
Resistance, $R_{DS(on)}$	6 Ω	0.085 Ω

In this work, a piezoelectric thin-film is bonded to the cantilever structure (Fig. 3) to provide a reference signal of the displacement cycle, in order to determine when the gate drive signal needs to be disabled. This ensures that during the negative voltage period the switch remains open, and also provides important power savings by reducing the gate drive losses and the quiescent power consumption. A similar solution was reported in [16] for a piezoelectric energy harvester. The piezoelectric sensor element is suitable for low power applications as no additional power supply is required.

Fig. 9 shows the measured converter output power for the four device options in half-wave boost rectifier configuration (Fig. 6 c), as the load is swept from 100 Ω to 15 k Ω . At each load impedance point, the duty ratio is varied so that the rms output voltage is maximized, corresponding to maximum average output power. This mimics the behavior of an idealized maximum power point tracking control circuit at steady-state conditions. The bidirectional MOSFET circuit is seen to provide the most output power, closely followed by the JFET and single MOSFET. The latter benefits from the harvester output voltage being low, below 0.5 V_{pk} , as its parasitic body-drain diode is not sufficiently forward biased to allow significant current to flow.

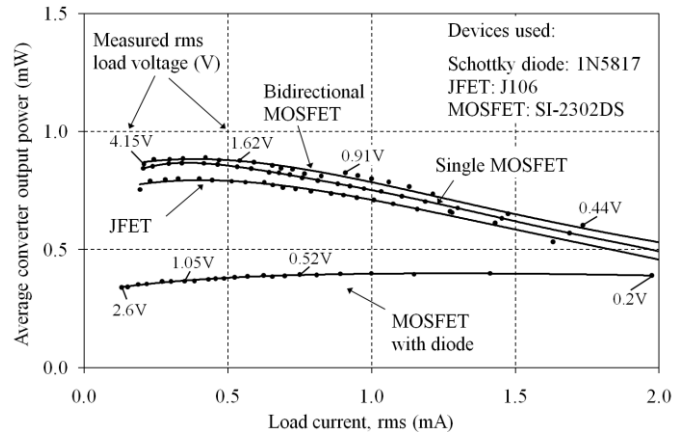


Figure 9. Average output power of half-wave boost rectifier with 1) JFET, 2) MOSFET with Schottky diode, 3) single n-type MOSFET, and 4) bidirectional MOSFET switch options. Source vibration is 6 m/s^2 at 59.4 Hz.

The devices in this experiment are controlled from externally powered gate drive circuitry. This connects the gate to the output of an arbitrary waveform generator during the positive half-cycle and shorts the gate to the source during the negative period. The results shown therefore do not include gate switching losses, or the quiescent power consumption of the gate drive circuit. It is interesting to note that taking account of the gate charging losses for the bidirectional MOSFET (52 μW) and the single MOSFET (20 μW) renders the two circuits approximately equivalent at this vibration level. Furthermore, the complexity of the gate drive circuitry, due to the additional requirement of non-ground-referenced gate signal, favors the single transistor design. The gate switching losses of the JFET and bidirectional MOSFET topology are approximately equal; however the JFET’s higher conduction losses and lower harvester utilization result in lower output power levels.

In the following sections, the bidirectional MOSFET is used as this offers a common active front-end for both half- and full-wave boost rectifier circuits (Fig. 10). The same active, boosting front-end topology can also be applied to the split-capacitor based converter topology in [9], which can be considered as an active front-end connected to a passive full-wave voltage doubler circuit.

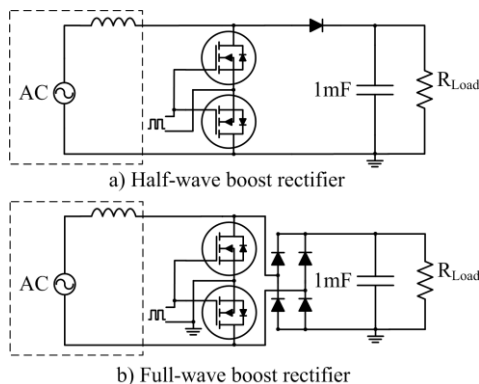


Figure 10. Boost rectifier circuits using bidirectional MOSFET.

B. Harvester Utilization

The average harvester output current, and inherently the apparent input resistance of the converter, is affected by the switching frequency, the duty ratio, the input and output voltages, and the load current. These factors also determine whether or not the inductor current discharges to zero while the switch is off, that is whether the converter is operating in discontinuous (DCM) or continuous current mode (CCM). Furthermore, multiple conduction modes can exist within one half-cycle, as illustrated in Fig. 2, thus varying the apparent resistance nonlinearly over time.

The effect on the harvester utilization of varying the duty ratio is measured (see Fig. 11 and Fig. 12) by sweeping the load resistance from 100 Ω to 20 kΩ at given duty ratios, and recording the changes in the generated power against load current. The converter’s output power is also captured at each measurement point. The converter input power traces show that by varying the duty ratio of the boost converter, the generated power can be kept approximately constant within the examined range of output current. The results also show that the harvester utilization of the full-wave boost rectifier is significantly better than that of the half-wave boost rectifier. In the full-wave case, the maximum generated power remains just under 1.4 mW for the full range of load currents. This corresponds to over 90% utilization of the maximum extractable harvester power of 1.42 mW (Fig. 5). In contrast, the input power measured for the half-wave circuit remains below 1.1 mW, and the harvester utilization around 77%, showing good agreement with the maximum power extracted with the ideal half-wave rectifier into a purely resistive load.

C. Converter efficiency

The harvester utilization must be considered in conjunction with the converters’ power efficiency to evaluate the overall harvesting system efficiency. Therefore, corresponding average converter output power (Fig. 13) and input power (Fig. 11 and Fig. 12) is measured in order to determine efficiency. In Fig. 11, the RMS output voltage corresponding to a single operating point close to the maximum average input power is shown for four different duty ratios. The data for the full-wave rectifier has been obtained from one experiment, that for the half-wave circuit from two experiments under the same conditions.

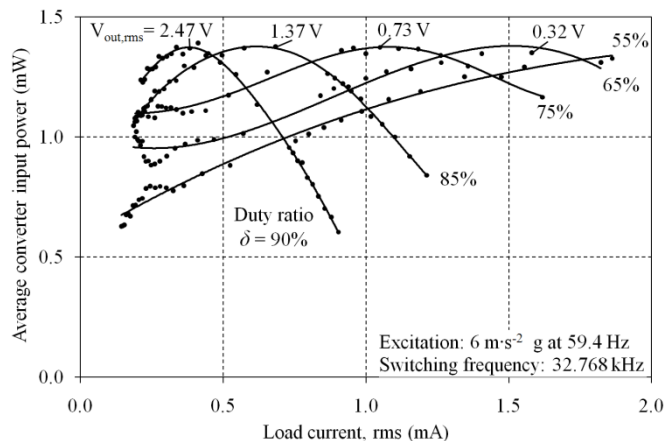


Figure 11. Input power versus load current for full-wave boost rectifier

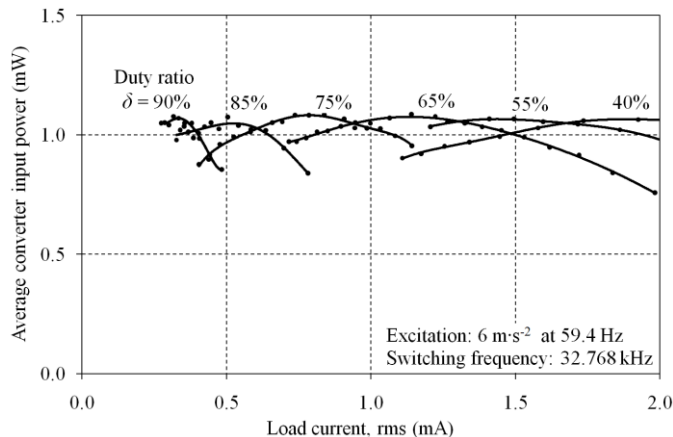


Figure 12. Input power versus load current for half-wave boost rectifier

Fig. 13 presents the output power data for both circuits as envelopes containing the power maxima for each duty ratio, operating points that would be achieved with appropriate control. The results neglect the gate switching losses as well as the quiescent power overhead of gate drive circuitry. The apparent converter output power for the full-wave boost rectifier exceeds that of the half-wave circuit by approximately 20 % at high duty ratios. Referring to Fig. 11-13, the apparent conversion efficiency of the half-wave boost circuit is in the range of 80–90% not including the gate drive losses. In comparison with this, the maximum efficiency of the full-wave rectifier circuit is lower at 75%. Diode conduction losses are significantly higher for the full-wave topology due to the higher number of conducting diodes.

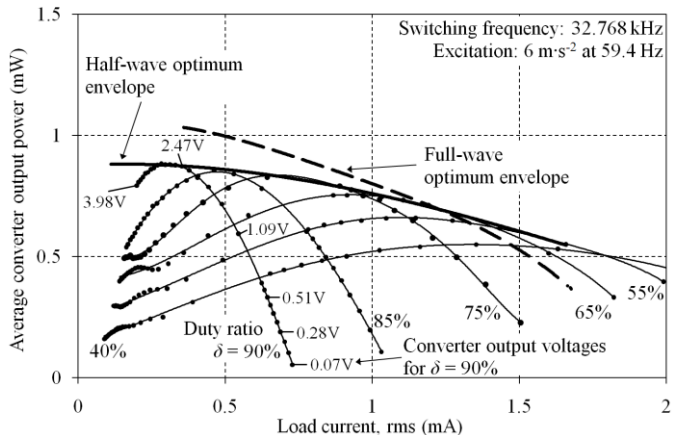


Figure 13. Average converter output power versus load current for half- and full-wave boost converter at varying duty ratio, as a function of load current.

These losses are also the main reason for the decreasing output power at increased load current, and why half-wave boost rectifiers deliver higher power above 1.35 mA.

At a fixed excitation level of 6 m/s^2 , the resulting overall system efficiency using a full-wave boost rectifier circuit is nevertheless higher than for the half-wave topology, due to the higher harvester utilization.

V. ANALYSIS OF COMPONENT LEVEL POWER LOSSES

As shown in Section IV, the maximum harvester utilization of the full-wave boost rectifier that can be achieved is significantly higher than for the half-wave topology. This difference is reduced when the overall system efficiency is considered, as a result of better conversion efficiency in the case of the half-wave circuit. The previous measurements ignore the gate drive and control circuit power overhead, as well as losses incurred during the commutation of the gate voltage. These losses become more critical, the lower the available power is. This section analyses these losses with decreasing available power; for this work the harvester excitation is swept, although in practice the reduced power could be a result of reduced harvester volume.

A component level power loss study is carried out at five excitation amplitudes: 1.5 m/s^2 , 2 m/s^2 , 4 m/s^2 , 6 m/s^2 , and 7 m/s^2 , where the maximum extractable powers are $141 \mu\text{W}$, $252 \mu\text{W}$, $696 \mu\text{W}$, 1.42 mW , and 1.92 mW respectively. At conditions ($10 \text{ k}\Omega$ load, 90% duty ratio, and 32.768 kHz) where the converter output power is near its maximum, input current, input voltage, output current and output voltage waveforms of at least two complete cycles are captured for the analysis. In practical systems, the converters should be operated close to this duty ratio, in order to maximize the output power into the storage capacitor. Typically, a secondary power converter situated between the energy storage element and the load circuitry regulates the load voltage to a specific required value.

Switching losses due to the following processes are considered: The charging of the diode's junction capacitance C_T to the reverse voltage when the device becomes reverse biased; the charging of the transistors' source-to-drain capacitances C_{DS} to the drain-to-source voltage V_{DS} when the devices turn off; the charging of the gate-to-drain capacitance C_{GD} from the gate voltage V_{GS} to V_{DS} at turn off; and the charging of the gate-to-source capacitance C_{GS} to V_{GS} via a resistive path. The last two losses are included in the gate charging losses combined with the losses due to the gate leakage current. Reverse recovery losses due to the recovery of the built up charge around the p-n junction is not significant in Schottky diode devices, however, reverse current to build up the depletion region as the diode is reverse biased is significant [17].

Conduction losses are incurred within the MOSFETs during the devices' ON period and within the diodes during the OFF period while they are forward biased. Further losses that are considered include the reverse leakage current of the diodes, power lost due to the equivalent series resistance and leakage of the energy storage capacitor, and the quiescent consumption of the gate-driver and control circuits. The power losses associated with the storage element are not expressed explicitly but shown as part of the remaining conversion losses. As no specific gate drive and control circuit was implemented, the power consumption overhead for this can only be estimated. Based on the commercially available low power boost converter chip, LTC3525L-3, the quiescent power is estimated to be $21 \mu\text{W}$ ($7 \mu\text{A}$ from a 3 V supply). The power consumption is assumed to be reduced to $0.3 \mu\text{W}$ when the unit is disabled and enters shut-down. This reduced power loss is used for the negative voltage half-cycle for the half-wave boost rectifier circuit.

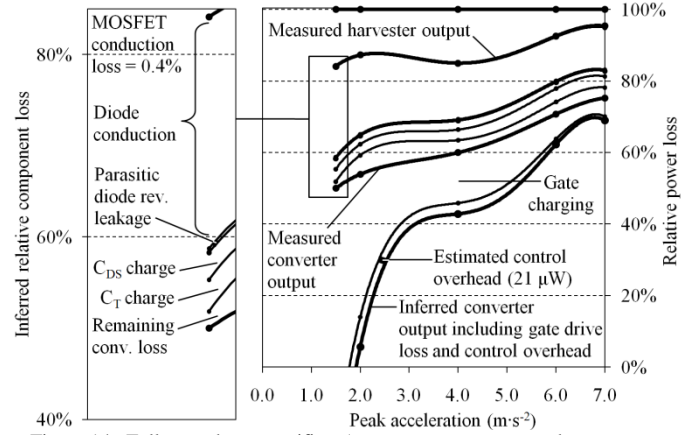


Figure 14. Full-wave boost rectifier: Average output power and component losses normalized to the maximum achievable power versus the magnitude of source vibration. Switching frequency is 32.768 kHz , duty ratio is 90% , and the load resistance is fixed at $10 \text{ k}\Omega$.

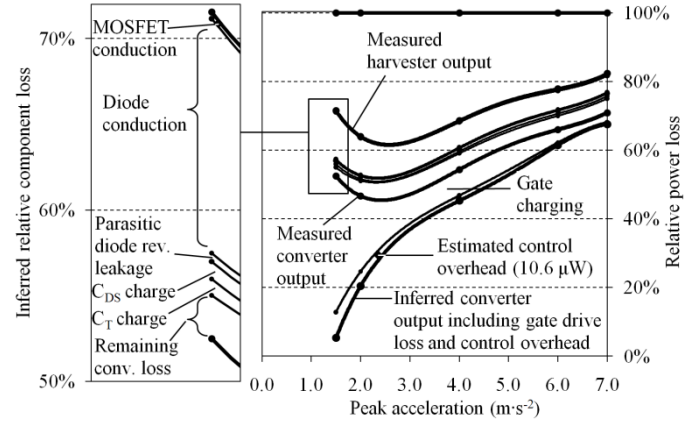


Figure 15. Half-wave boost rectifier: Average output power and component losses normalized to the maximum achievable power versus the magnitude of source vibration. Switching frequency is 32.768 kHz , duty ratio is 90% , and the load resistance is fixed at $10 \text{ k}\Omega$.

TABLE II. CONVERTER OUTPUT VOLTAGE

Excitation Level	Measured converter output voltage (rms)	
	Full-wave boost rectifier	Half-wave boost rectifier
1.5 m/s^2	0.840 V	0.861 V
2.0 m/s^2	1.116 V	1.085 V
4.0 m/s^2	2.043 V	1.945 V
6.0 m/s^2	3.161 V	3.052 V
7.0 m/s^2	3.793 V	3.682 V

Fig. 14 and Fig. 15 show results for full- and half-wave topologies respectively. The inferred power losses are presented normalized to the maximum extractable harvester power at each excitation magnitude. Diode conduction loss is the main contributor to the overall power loss for both topologies, however, this power penalty is significantly higher for the full-wave circuit which has two diodes per current path. The calculated gate switching losses are also significant, whilst the conduction losses of the MOSFETs are negligible. For excitation levels below 4 m/s^2 , corresponding to power levels below $700 \mu\text{W}$, the half-wave converter is shown to become more effective. In fact, at the lowest excitation, where the maximum available power is $141 \mu\text{W}$, the full-wave topology is not feasible as the power overheads of the gate drive circuit and the gate switching losses exceed the converter output power, forcing the inferred total output power into the negative. The half-wave boost rectifier circuit is seen to extract power down to a lower excitation level than its full-wave equivalent. This cut-off point,

and indeed the difference between the harvester utilization achieved with the two topologies is dependent on the mechanical characteristics of the harvester [12], however, the overall trends remain valid.

The analysis shows a high ratio between the MOSFETs' gate charging losses to forward conduction loss; a higher performance can be achieved with a smaller active device area that translates into lower gate capacitances at the expense of higher on-state resistance. The 2N7002 has a typical C_{iss} of 20 pF, and an $R_{ds(on)}$ of approximately 1.4 Ω at a gate voltage of 2.7 V. The measured converter input power at 1.5 $m\cdot s^{-2}$ excitation is 77 μW , which shows that the harvester utilization is less. The output power is also reduced from 74 μW to 43.8 μW . However, the gate switching losses are significantly reduced, from 55.9 μW to 7.1 μW resulting in a useful output power of 26.1 μW when the estimated quiescent power consumptions are considered. This shows an overall system efficiency improvement of over 10%, from 5.26% to 18.53%.

VI. CONCLUSIONS

Experimental results demonstrate the successful operation of boost rectifier circuits without a discrete inductor down to 141 μW of available harvester power. The maximum extractable harvester power using a purely resistive AC load is 1.42 mW at 6 $m\cdot s^{-2}$ amplitude excitation. The achievable power is reduced to 1.12 mW if the generator is only loaded during half of the displacement cycle. Using the example of passive half- and full-wave Schottky diode rectifier circuits with a smoothed output voltage, the effect of the conversion efficiency of the interfacing power electronics circuits is illustrated; the half-wave passive rectifier is shown to have more than twice the average output power of the full-wave circuit.

A bidirectional MOSFET, formed by a common source connected n-type MOSFET pair, is selected as the active front-end for both half- and full-wave boost rectifier circuits. Single JFET, and n-type MOSFET based half-wave topologies offer comparable output power performance and should be further investigated in the future with a particular focus on the trade-offs between gate switching losses, gate drive circuit complexity and current leakage during the unloaded half cycle.

Full-wave boost rectifier circuits are shown to be capable of presenting a near optimum damping condition for the energy harvester, resulting in over 90% harvester utilization at 6 $m\cdot s^{-2}$ source excitation. The half-wave boost rectifier topology has worse utilization, in the range of 75%, when compared to the full-wave circuit, but offers improved power conversion efficiencies, in the range of 80–90% near 1 mW input power level, when gate switching losses and gate drive and control circuit power overheads are ignored. The effects of these additional power penalties are considered in a component-level loss analysis at five different excitation magnitudes. As the maximum extractable harvester power is reduced, the benefits of full-wave operation are negated by the lower conversion efficiency and the higher gate drive circuit power overheads. It is shown experimentally, that for the particular harvester used in this work, the point where half-wave boost rectifier circuit becomes more effective is around 700 μW of extractable power. The high ratio between the MOSFETs' switching and conduction losses shows that the useful output power can be increased by using a device with smaller active area. At a maximum available harvester power of 141 μW ; the useful output power is increased to 26.1 μW from 7.4 μW when the average quiescent power losses are estimated to be 10.65 μW . The relatively high diode conduction losses indicate that synchronous topologies could potentially offer better conversion efficiencies, and thus increased useful output power, at the cost of added switching losses.

Future work should consider the effect of varying switching frequency as well as duty ratio to achieve optimum damping. Low power control techniques, including skip mode and hysteretic control,

should also be investigated. The limitations of stray inductance based circuit topologies should be quantified, especially for microscale harvesting systems where the coil resistance is more significant.

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